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Synplicity FPGA Synthesis User Guide

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To set up the Intel® Quartus® Prime software to run the Synplify software, do the following: On the Tools menu, click Options. In the Options dialog box, click EDA Tool Options and specify the path of the Synplify or Synplify Pro software under Location of Executable.

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The tutorial is designed to walk you through the Synplify Pro design flow using some typical tasks and familiarize you with the user interface. The tutorial design is an 8-bit micro controller.

## [Synopsys FPGA Synthesis](#)

- Synplify Premier tool to improve timing closure with Graph-based Physical Synthesis. Graph-based Physical Synthesis provides design stability, accurate timing correlation, minimal design iterations, and great timing performance. Single-Chip ASIC Verification Synplify Premier supports single-chip ASIC

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verification with: • Gated Clock Conversion

## Synplify Quick Start for Xilinx

Synplify Pro ® Reference Manual February 2004 Synplicity, Inc. 600 West California Avenue Sunnyvale, CA 94086 (U.S.) +1 408 215-6000 direct (U.S.) +1 408 222-0263 fax

## Synplify Pro Reference Manual

Devices and IP used outside of data sheet limits, or in a manner inconsistent with general instructions in the User Guide. Modifications to cores generated by Coregen are not supported. For design or coding assistance, contact your Authorized Distributor or Sales Representative.

## Support - Xilinx

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## Synplify Premier - Xilinx

To add to my last answer, you can refer to "Synopsys FPGA Synthesis User Guide" (fpga\_user\_guide.pdf) and search for Section "Incorporating Vivado IP". -vivian Don't forget to reply, kudo, and accept as solution.

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